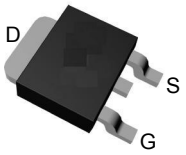
SL403

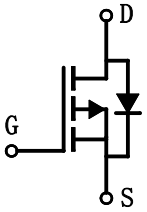
P-Channl Enhancement Mode MOSFET

- -30V/-70A
- $R_{DS(ON)}$=5.1mΩ (typ) @V_{GS}=-20V
  $R_{DS(ON)}$=6.2mΩ (typ) @V_{GS}=-10V
- 100% UIS & RG Tested
- Reliableand Rugged
- Lead Freeand Green Devices Available
  (RoHS Compliant)

Pin Configuration



Top View of TO-252-3



Applications

- Power Management for Industrial DC/DC Converters

Absolute Maximum Ratings (T_A= 25°C unless otherwise noted)

Symbol	Parameter		Rating	Unit
Common Ratings				
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±25	
I_D	Continuous Drain Current [G]	Tc=25°C	-70	A
		Tc=100°C	-55	
I_{DM}	Pulsed Drain Current [C]	Tc=25°C	-200	
I_{DSM}	Coutinuous Drain Current	T_A=25°C	-15	A
		T_A=70°C	-12	
P_D	Power Dissipation [B]	T_C=25°C	90	W
		T_C=100°C	45	
T_{STG}, T_j	Storage Temperature Range		-55 to 175	°C
P_{DSM}	POwer Dissipation [A]	T_A=25°C	2.5	W
		T_A=70°C	1.6	
I_{AS}	Single pulsed avalanlce Current [C]		-50	A
E_{AS}	Single pulsed avalanlce energy [C]	L=0.1mH	125	mJ
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Staedy-State	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient [AD]	t ≤10S	20	
		Staedy-State	50	

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
		T_J=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±25V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA	-1.5	-2.5	-3.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-200			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-20V, I_D=-20A		5.1	6.2	mΩ
		T_J=125℃		7.6	9.2	
		V_{GS}=-10V, I_D=-20A		6.2	8	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-20A		42		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current[G]				-70	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz	2310	2890	3500	pF
C_{oss}	Output Capacitance		410	585	760	pF
C_{rss}	Reverse Transfer Capacitance		280	470	660	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.9	3.8	5.7	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-20A	40	51	61	nC
Q_{gs}	Gate Source Charge		10	12	14	nC
Q_{gd}	Gate Drain Charge		10	16	22	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=0.75Ω, R_{GEN}=3Ω		16		ns
t_r	Turn-On Rise Time			12		ns
$t_{D(off)}$	Turn-Off DelayTime			45		ns
t_f	Turn-Off Fall Time			22		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-20A, dI/dt=100A/μs	14	18	22	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-20A, dI/dt=100A/μs	9	11	13	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

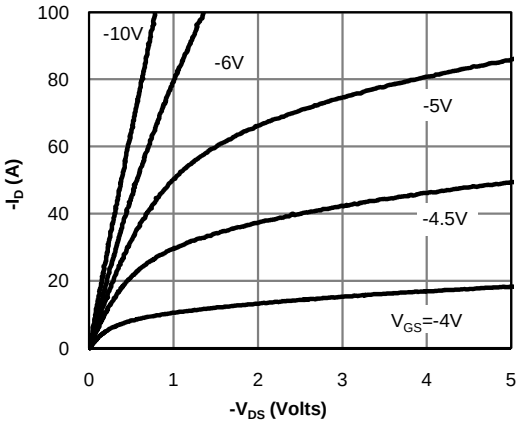


Fig 1: On-Region Characteristics (Note E)

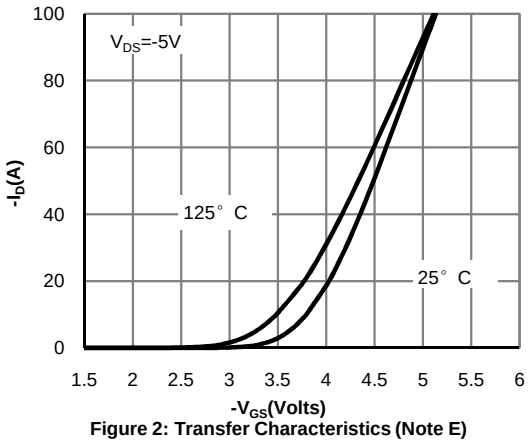


Figure 2: Transfer Characteristics (Note E)

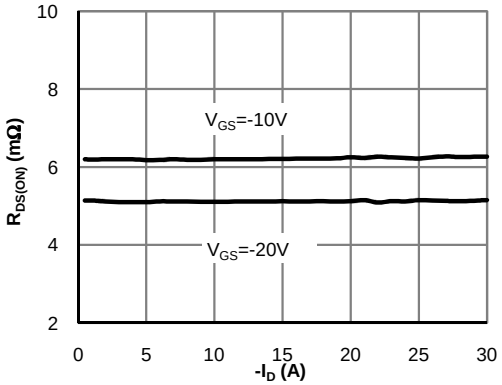


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

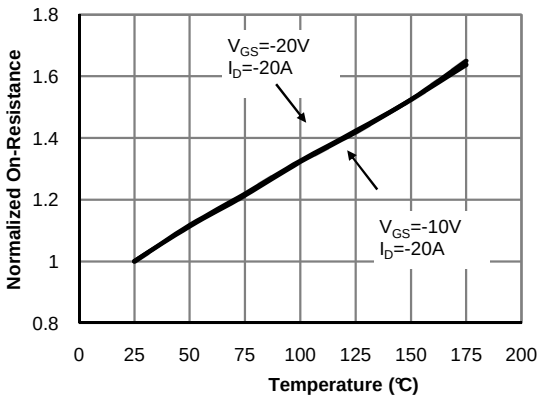


Figure 4: On-Resistance vs. Junction Temperature (Note E)

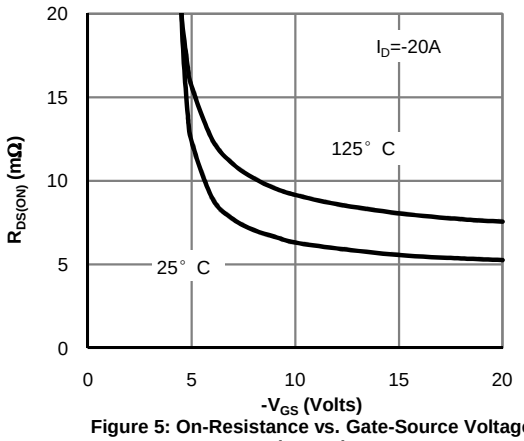


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

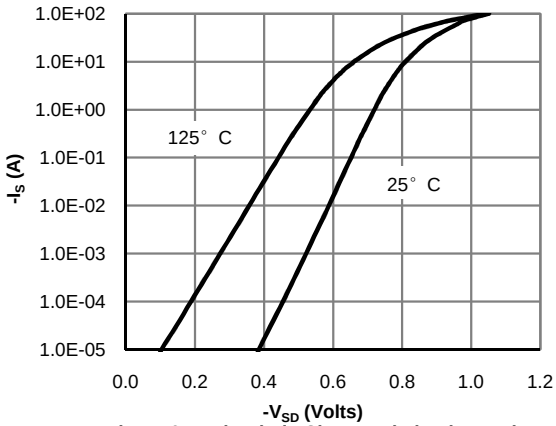


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

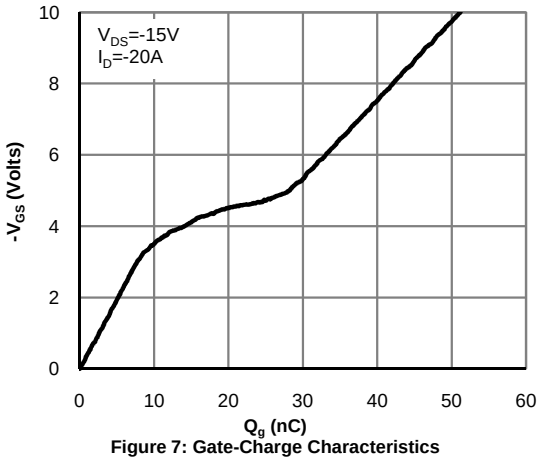


Figure 7: Gate-Charge Characteristics

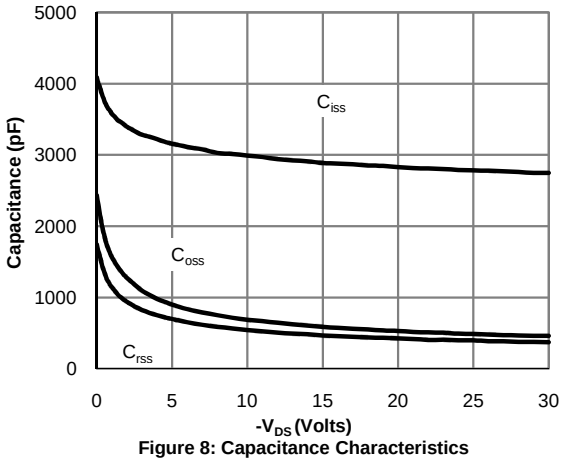


Figure 8: Capacitance Characteristics

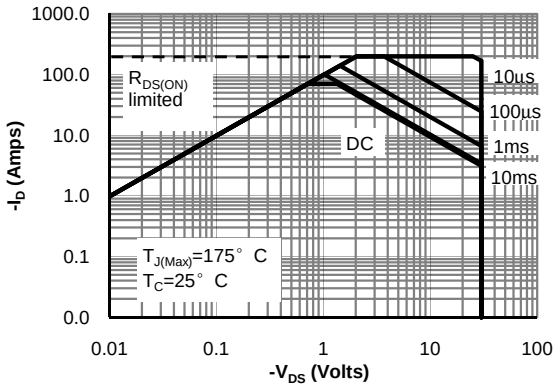


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

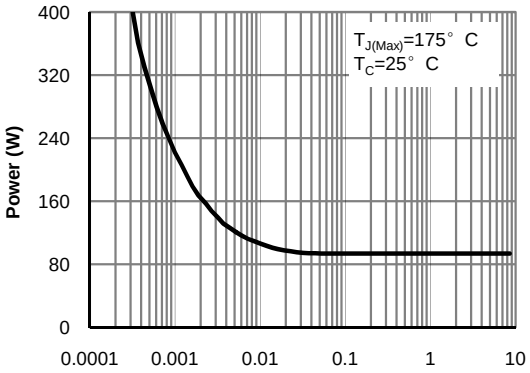


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

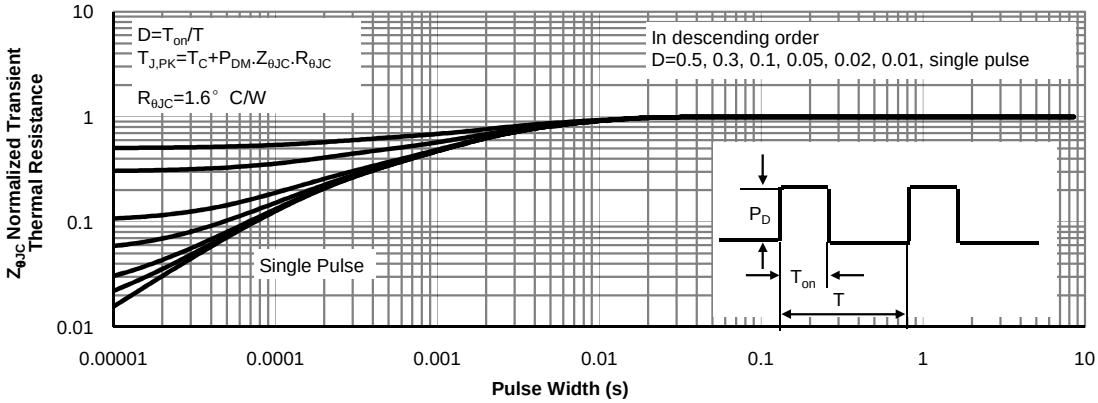


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

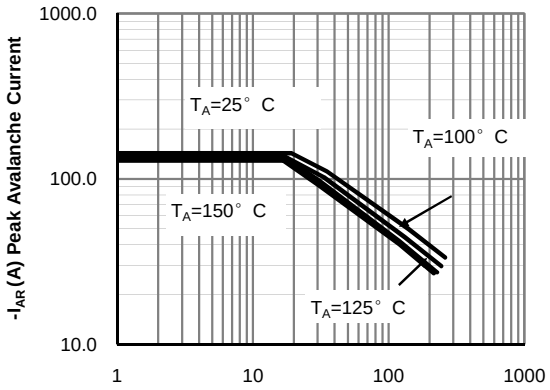


Figure 12: Single Pulse Avalanche capability (Note C)

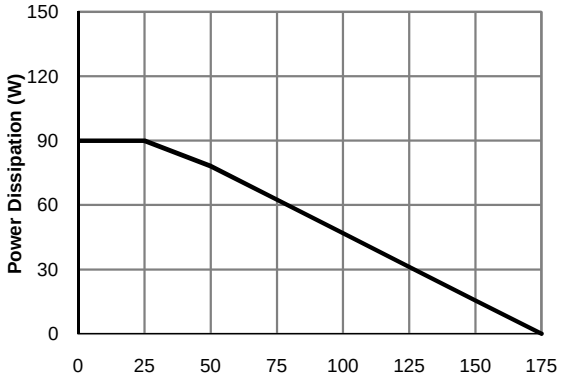


Figure 13: Power De-rating (Note F)

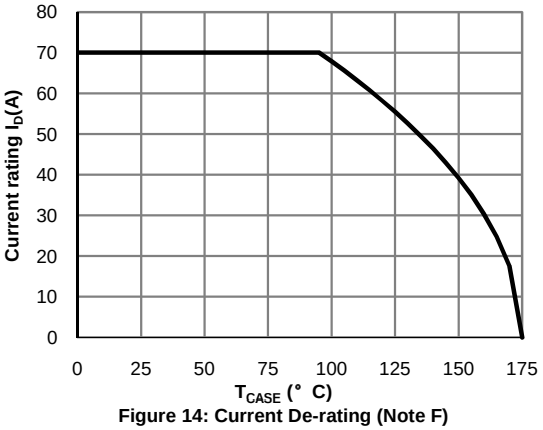


Figure 14: Current De-rating (Note F)

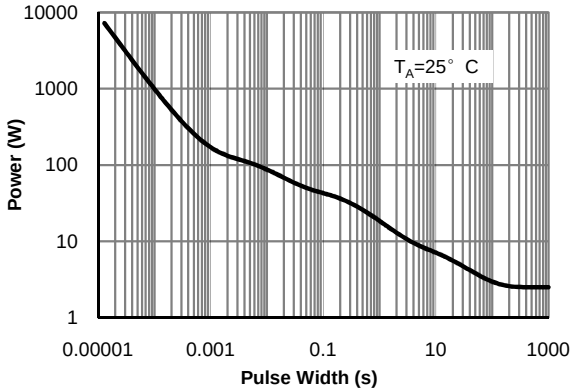


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

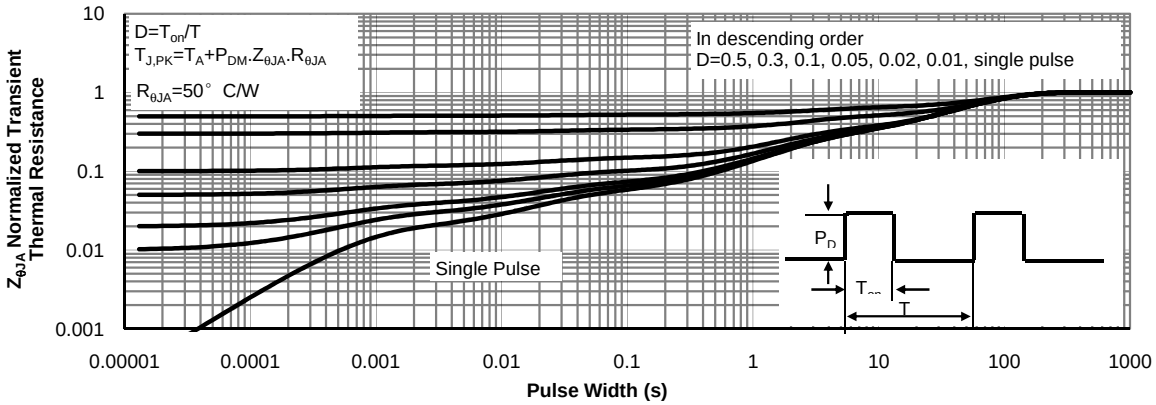
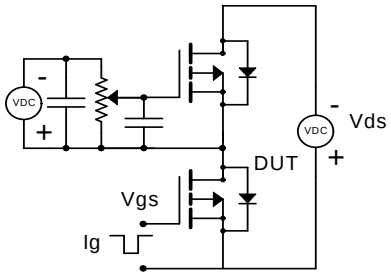
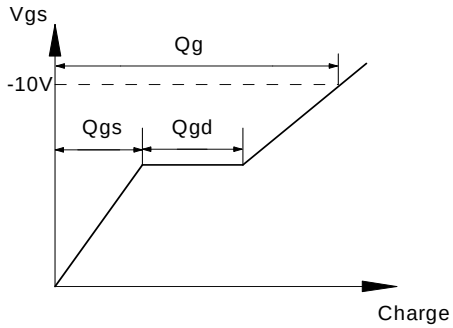


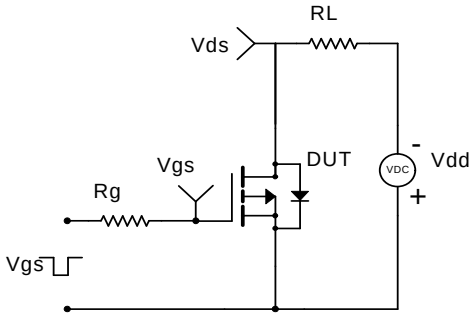
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

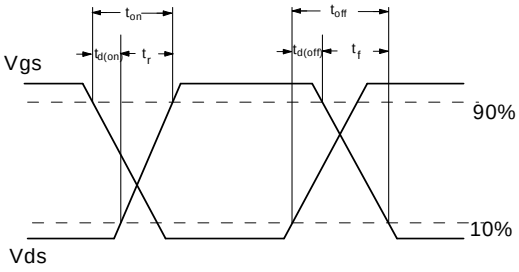
Gate Charge Test Circuit & Waveform



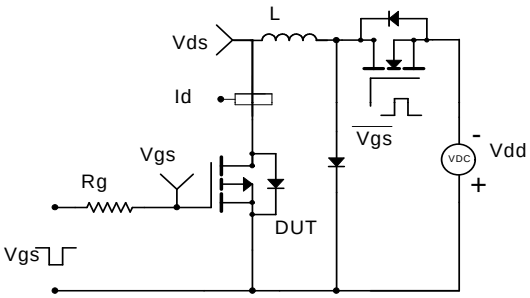


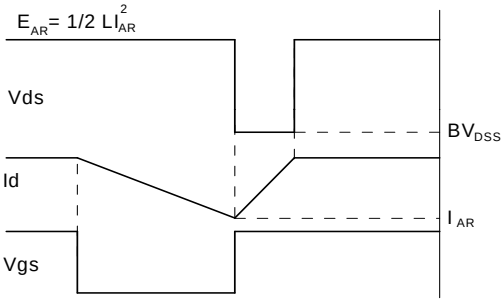
Resistive Switching Test Circuit & Waveforms



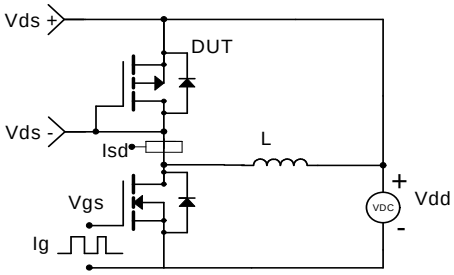


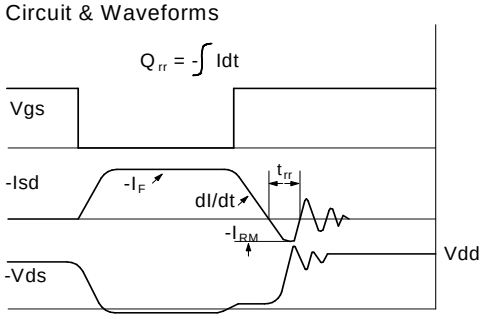
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





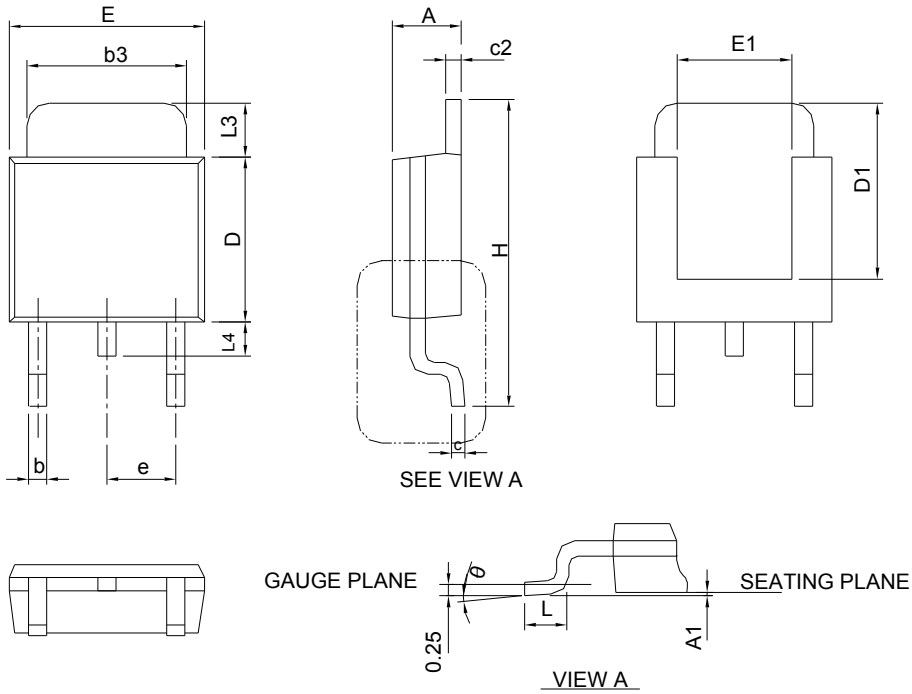
Diode Recovery Test Circuit & Waveforms





Package Information

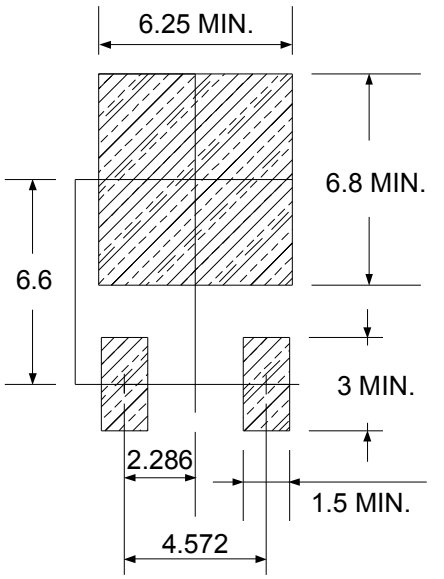
TO-252-3



SYMBOL	TO-252-3			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	-	0.13	-	0.005
b	0.50	0.89	0.020	0.035
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	0.90	1.78	0.035	0.070
L3	0.89	2.03	0.035	0.080
L4	-	1.02	-	0.040
θ	0°	8°	0°	8°

Note : Follow JEDEC TO-252 .

RECOMMENDED LAND PATTERN



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